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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/487,259		Sasaki Shigeyuki	1035-243	2949

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EXAMINER
MAI, ANH D

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/487,259	SHIGEYUKI, SASAKI	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *6-8 and 20-42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 9-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12,17* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 30, 2002 has been entered.

Status of the Claims

2. Claims 1-42 are pending. Claims 6-8 and 20-42 have been withdrawn. Action on merits of claims 1-5 and 9-19 follows.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: METHOD FOR MANUFACTURING A SEMICONDUCTOR DICE BY PARTIALLY DICING THE SUBSTRATE AND SUBSEQUENT CHEMICAL ETCHING.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3-5, 9, 10 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Tayakashiki et al. (JP 03-270156) of record.

Tayakashiki teaches a manufacturing method for a semiconductor device as claimed including:

semi-full dicing a semiconductor wafer (10) so as to leave a dicing residual portion with a predetermined thickness between devices (15) on the semiconductor wafer (10);

forming a protective layer (13) having a chemical etching resistant property on an element formation (front) face of the semiconductor wafer (10); and

chemically etching the semiconductor wafer (10) having the protective layer (13) formed on the element formation (front) face from the rear face side so as to polish the rear face of the semiconductor wafer (10), so as to remove the dicing residual portion to divide the semiconductor wafer (10) into individual semiconductor chips (15), and so as to remove damaged areas in a cut face of the semiconductor wafer (10) resulting from the semi-full dicing process. (See Abstract, Fig. 1).

With respect to claim 3, the process of Tayakashiki further includes: removing the protective layer (13) from the semiconductor chips after the chemical etching step, thus forms individual chips (15).

With respect to claim 4, the semi-full dicing step of Tayakashiki includes: subjecting the semiconductor wafer (10) to semi-full dicing from the element formation (front) face so as to leave a dicing residual portion with a predetermined thickness on the rear face side of the semiconductor wafer (10).

With respect to claim 5, the protective layer (13) of Tayakashiki is formed on the element formation (front) face of the semiconductor wafer (10).

With respect to claim 9, the protective layer (13) of Tayakashiki is a film.

With respect to claim 10, the protective layer (13) of Tayakashiki is a chemical etching resistant film of ultraviolet separation type, which has a reduction in adhesive strength upon irradiated with ultraviolet rays.

With respect to claim 12, the protective layer (13) of Tayakashiki is a chemical etching resistant film of a sticking type, which has an adhesive strength that allows the individually divided semiconductor chips to be separated from the protective layer one by one.

5. Claims 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tayakashiki '156 as applied to claim 1 above, and further in view of applicant admitted prior art (JP. 07-022358) of record.

Tayakashiki teaches all of the features of the claim with the exception of explicitly disclosing a testing step prior to the semi-full dicing.

However, the admitted prior art teaches that prior to dicing, the semiconductor wafer (101) is subjected to an electrical test by probing. (See page 2, lines 1-8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to perform testing prior to semi-full dicing the semiconductor wafer (10) of Tayakashiki as taught by the admitted prior art to identify the bad chips prior to dicing.

6. Claims 11 and 13-19 are further rejected under 35 U.S.C. 103(a) as being unpatentable over Tayakashiki '156 as applied to claim 1 above, and further in view of Usami et al. (U.S. Patent No. 5,893,746).

With respect to claim 11, Tayakashiki teaches forming a protective layer (13) having a chemical etching resistant property on the semiconductor wafer (10).

Thus, Tayakashiki is shown to teach all of the features of the claim with the exception of the protective layer is of a thermal type which reduces the adhesive strength upon exposing to heat.

However, Usami teaches the protective layer (203) which lowers adhesive properties by irradiation of ultraviolet (UV) light or by application of heat are well known in the art to temporarily adhere to the semiconductor substrate for dicing process.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the protective layer (3) of Tayakashiki using the adhesive tape of thermal type as taught by Usami for easy removal of the diced chips.

With respect to claim 13, the protective layer (4) of Usami is held by a protective layer holding means (101) with an uniform tension.

With respect to claim 14, the uniform tension of Usami is maintained on the protective layer (107') by a protective layer holding means (101') placed on a face of the protective layer that is opposite to the face of the protective layer (107') on which the semiconductor wafer (105) is affixed.

With respect to claim 15, the uniform tension of Usami is maintained on the protective layer (107) by a protective holding means (101) placed on the same surface of the protective layer (107) as the semiconductor wafer (105).

With respect to claim 16, the protective holding means (101) of Usami having a chemical etching resistance property is placed on a peripheral portion of the protective layer (107) so as to surround the entire circumference of the semiconductor wafer (105).

With respect to claim 17, the protective layer holding means (101) of Usami has a ring shape with a flat bonding face for bonding with the protective layer (107).

With respect to claim 18, the manufacturing of Tayakashiki in view of Usami include the protective layer (107) being placed on the protective holding means (101).

Thus, Tayakashiki and Usami teach all of the features of the claim with the exception of explicitly disclosing a draining means for draining etchant during the chemical etching. Note that the specification contains no disclosure of either the *critical nature of the claimed draining means or any unexpected results arising therefrom*.

However, the dicing apparatus is known to includes dicing wheel and cooling means to cool the wheel and removing the dust created during the cut. Water or liquid are known cooling medium. Therefore, standing liquid in the dicing apparatus must be eliminate to prevent contamination. Thus, draining means is inherent of the apparatus.

With respect to claim 19, since shape of the holding means (101) of Usami is round therefore, any draining means formed in the holding means (101) should inherently extending in a radial manner.

Response to Arguments

7. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
May 16, 2003